UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,486	01/13/2006	Hyo-Kun Son	3449-0567PUS1	9185

2292 7590 10/07/2008

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
MIYOSHI, JESSE Y	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
10/07/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/564,486	SON, HYO-KUN	
	Examiner	Art Unit	
	JESSE Y. MIYOSHI	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33,34,36-44 and 46-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33,34,36-44 and 46-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 33, 34, 36-44, 46-50 are rejected under 35 U.S.C. 102(b) as being anticipated by the applicant provided prior art to Tanizawa et al. (EP 1063711; hereinafter "Tanizawa").

Re claim 33: Tanizawa teaches (e.g. paragraph 110 and figure 1) a light emitting diode (LED), comprising: a first gallium nitride layer (**5**); an $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer (**6**) formed over the first gallium nitride layer (**5**); an active layer (**7**) formed over the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer (**6**); and a second gallium nitride layer (**9**) formed over the active layer (**7**); wherein the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi- layer (**6**) has a plurality of pits formed thereon (as stated on page 7, lines 20-22 of the specification, the pits are naturally occurring, therefore Tanizawa would inherently be provided with pits).

Re claim 34: Tanizawa teaches the LED wherein the active layer (**7**) comprises an InGaN/InGaN structure of a multi-quantum well structure (**7**, multi quantum well structure; e.g. paragraph 110).

Re claim 36: Tanizawa teaches the device wherein the number of the pits is 50 or less per area of 5μm X 5μm. The formed pits are a result of the composition of the structure as disclosed in claim 33, therefore, since the structure recited in the prior art is

substantially identical to that of the claim, claimed properties are presumed to be inherent. See MPEP 2112.01(i).

Re claim 37: Tanizawa teaches the LED wherein the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer is formed to have a super lattice structure (superlattice structure **6**).

Re claim 38: Tanizawa teaches the LED wherein each layer of the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer has a thickness of 1-3000Å (superlattice **6** have layers not greater than 100Å; e.g. paragraph 114).

Re claim 39: Tanizawa teaches the device wherein the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer has a photoluminescence characteristic of a yellow band intensity/N-doped GaN intensity ratio of 0.4 or below. Since the structure recited in the prior art is substantially identical to that of the claim, claimed properties are presumed to be inherent. See MPEP 2112.01(i).

Re claim 40: Tanizawa teaches the active layer (**7**) being directly formed on the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer (**6**).

Re claim 41: Tanizawa teaches the LED wherein the LED is blue LED (pure blue light of 470nm; e.g. paragraph 421).

Re claim 42: Tanizawa teaches (e.g. paragraph 110 and figure 1) a method for manufacturing a light emitting device, the method comprising the steps of: forming an N-type gallium nitride layer (**4**); forming an $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer (**6**) above the N-type gallium nitride layer (**4**), the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer (**4**) including layers of first and second growth temperatures (GaN and $In_{0.13}Ga_{0.87}N$ layers formed at different temperatures, temperature lowered to 800°C to form InGaN layer of superlattice; e.g.

paragraph 410); forming an active layer (**7**) above the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer (**4**); and forming a P-type gallium nitride layer (**9**) above the active layer (**7**), wherein the active layer (**7**) is grown at a temperature lower than the first and second temperatures (active layer has a higher In content, $In_{0.3}Ga_{0.7}N$, therefore is grown at a lower temperature less than or equal to 800˚C; e.g. paragraph 420); and wherein the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer (**4**) has a plurality of pits formed thereon (as stated on page 7, lines 20-22 of the specification, the pits are naturally occurring, therefore Tanizawa would inherently be provided with pits).

Re claim 43: Tanizawa teaches the method wherein the active layer is grown at 600~800 °C (active layer GaN barrier layer is grown at 800˚C, therefore, InGaN well layer is grown at a temperature less than 800˚C; e.g. paragraph 420).

Re claim 44: Tanizawa teaches the method wherein the active layer comprises an InGaN/InGaN structure of a multi-quantum well structure (**7**, multi quantum well structure; e.g. paragraph 110).

Re claim 46: Tanizawa teaches the device wherein the number of the pits is 50 or less per area of 5μm X 5μm. The formed pits are a result of the method of making structure as disclosed in claim 42, therefore, since the structure recited in the prior art is formed substantially identical to that of the claim, claimed properties are presumed to be inherent. See MPEP 2112.01(i).

Re claim 47: Tanizawa teaches the method wherein the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer is formed to have a super lattice structure (superlattice structure **6**).

Re claim 48: Tanizawa teaches the method wherein each layer of the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer has a thickness of 1-3000Å (superlattice **6** have layers not greater than 100Å; e.g. paragraph 114).

Re claim 49: Tanizawa teaches the device wherein the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer has a photoluminescence characteristic of a yellow band intensity/N-doped GaN intensity ratio of 0.4 or below. Since the structure recited in the prior art is substantially identical to that of the claim, claimed properties are presumed to be inherent. See MPEP 2112.01(i).

Re claim 50: Tanizawa teaches the active layer (**7**) being directly formed on the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer (**6**).

Conclusion

3. Examiner's note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSE Y. MIYOSHI whose telephone number is (571)270-1629. The examiner can normally be reached on M-F 7:30AM-5:00PM EST. Alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/Jesse Miyoshi/